P.7: Installation and commissioning of compact Digital Low Level RF System for RF stations 5 & 6 of Indus-2

The Digital Low Level Radio Frequency (DLLRF) system is crucial part of the RF accelerating system in a synchrotron radiation source. In the Indus-2 storage ring, precise control of cavity voltage amplitude and phase at 505.8 MHz is essential for maintaining longitudinal beam stability, minimizing synchrotron oscillations, and ensuring reliable injection and stored beam operation. The DLLRF system continuously senses the cavity field, compares it with a reference, and dynamically corrects deviations through high-speed digital feedback implemented in FPGA hardware.

During the long shutdown period of December 2025- January 2026, a compact upgraded DLLRF system was installed and commissioned for RF Stations 5 and 6 of Indus-2. The upgrade involved replacement of discrete units with a compact and indigenously developed RF signal processing, automated synchronization features and enhanced protection mechanisms. The complete installed system is shown in Fig. P.7.1.

Fig. P.7.1: Compact DLLRF for Station 5 & 6 Installed in Indus-2

The cavity pickup signal at 505.8 MHz is first down-converted to an intermediate frequency (IF) of 21.075 MHz. For this purpose, a local oscillator (LO) frequency of 526.875 MHz is generated by the LO & Clock generation unit. The down-converted IF signal is digitized using high-speed ADCs, and digital IQ sampling is implemented within the FPGA.

In-phase (I) and quadrature-phase (Q) components are processed through a CORDIC algorithm to determine instantaneous amplitude and phase of the cavity field. Detected amplitude and phase are compared with the reference set values and Proportional – Integral (PI) controller is implemented in FPGA to generate the correction signals using DAC. This correction signal is up converted using I/Q modulator that drives RF amplifier and subsequently to the accelerating cavity, thereby closing the feedback loop and maintaining the required stability.

Key feature of the upgraded system is the integration of indigenously developed multi-channel up-down converter modules with high dynamic range and low phase noise performance. The LO & Clock unit, also developed indigenously, provides automated programming capability and synchronized clock distribution. This ensures low phase noise reference generation and flexible configuration. Digital filters are implemented in FPGA to suppress noise components present in the reference signals. This has significantly improved the amplitude and phase stability (Fig. P.7.2).

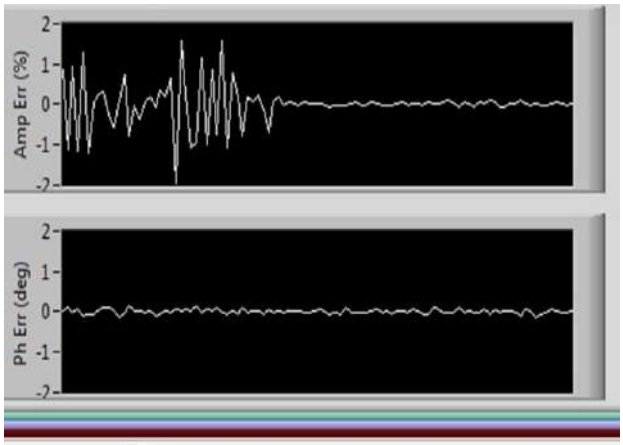

Fig. P.7.2: Screenshot of DLLRF GUI showing improved Amplitude error with filter switching

To ensure the operational safety, system reliability and enhanced fault detection capabilities a redundant interlock system and multi-channel power monitoring boards have been installed along with the DLLRF upgrade. These boards, developed indigenously, are capable of monitoring forward power, reflected power, cavity sense power, and reference power through multiple channels. It also has a pair of RF switches to enable rapid isolation of the drive in case of abnormal conditions. Few firmware upgradations have also been carried out including the calibration and auto synchronization feature.

The successful commissioning of the compact DLLRF systems for RF Stations 5 and 6 demonstrates improved amplitude and phase stability, enhanced noise immunity, updated firmware and strengthened protection mechanisms. The indigenous development of the up/down converter units, LO & Clock board, interlock modules, and monitoring electronics represents a significant technological achievement.

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