

Fig.A.5.1 : X-ray reflectivity pattern (dots) of short period W/Si Multilayer mirror along with fitting (redline)

polarization experiments and hard x-ray super mirrors for Indus 2. Development of short period multilayers is a prerequisite for the above mentioned goal.

Depositing these structures with good periodicity and low roughness is a technological challenge. At low period thicknesses ($< 2\text{nm}$), intermixing of layers reduces reflectivity significantly. If intermixing is not controlled, the desired performance from the multilayer structure would not be achieved.

We report deposition and characterization of short period W/Si and W/C multilayers using an in-house developed ion beam sputtering thin film deposition system. Base pressure in the chamber before deposition was 2×10^{-6} mbar and during the deposition was maintained at $\sim 4 \times 10^{-4}$ mbar. Before deposition, r.m.s roughness of each substrate was measured by grazing incidence x-ray reflectivity (GIXRR) technique on a reflectometer developed in house on a sealed tube with Cu target (8.05 keV).

Figure A.5.1 shows the reflectivity pattern of 20 layer

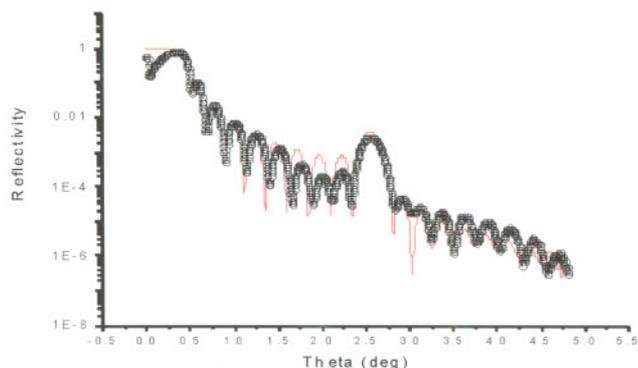


Fig. A5.2: X-ray reflectivity pattern (dots) of short period W/C Multilayer mirror along with fitting (red line)

pair W/Si multilayer mirror along with the best fit line. The estimated period thickness is 1.7 nm and the reflectivity of the Bragg peak was 0.09 % at 2.57° theta. The thickness of W layer was 1 nm with a roughness of 0.45 nm and of Si layer was 0.7 nm with a roughness of 0.6 nm. Reflectivity analysis also revealed that there is significant intermixing taking place at the interface of W and Si. Densities of W and Si layer have got considerably changed.

Figure A.5.2 shows reflectivity pattern of 10 layer pair W/C multilayer mirror along with the best fit line. In this case, the estimated period from the fitting was of 1.74 nm and the reflectivity of the Bragg peak was 0.28 % at 2.54° theta. The thickness of W layer was 1.04 nm with a roughness of 0.4 nm and of Si layer was 0.7 nm with a roughness of 0.5 nm. In this case no intermixing was observed and densities of W and C layer were as expected.

It can be seen from the above data that reflectivity of W/C multilayer mirror is much higher (0.28%) than of W/Si multilayer mirror (0.09%) of same period. The major reason for this is that the roughness of C layer is smaller than the roughness of Si layer and lower intermixing at W/C interface compared to W/Si. This development is very useful for our aim of developing hard x-ray super mirrors and normal incidence mirrors in water window region. Efforts are going on to further reduce the multilayer period.

Reported by
Sanjay Rai (sanjayrai@rrcat.gov.in) Arijeet Das, and
G. S.Lodha

A.6: Control Integration of Indus-2 BL-21 Front End

A beamline front end is typically the part of the beam line, which is inside the inaccessible, shielded ring area and connects the actual beam line housing the experimental station to the ring with needed regulating and controlling mechanisms for synchrotron beam and vacuum. Every front end has its local controls for facilitating local operations and procedures. Every front end also has local safety interlocks for ensuring safe operation of the front end. However, it is required to have co-ordinated operations with the machine controls to allow proper, safe and authorized use of the beam lines. Safety aspects related to radiation levels around the experimental area and vacuum in the ring as well as the front end are of primary concern. Proper use concerns the control of 'safety shutter', which allows the photon beam to the beam line and closely monitoring vacuum before opening the gate valves.

The control co-ordination concerns the permission to open gate valve 1 (GV1) in the front end, permission to open and close safety shutter (SS), withdrawing the permissions for SS and GV1 in case of unsafe conditions.



Fig.A.6.1 : Beam Line Front Ends GUI Panel with BL-21 Front End Controls Integrated.

Protection of ring vacuum is ensured by gate valves, designated GV0s, located at the periphery of Indus-2 ring. These GV0s separate the machine vacuum envelope from those of the beamlines. These are installed at the beginning of beamline front ends (BLFE). These pneumatic gate valves allow remote control and status monitoring through their controllers.

Front end controls for beam line 21 of Indus-2 were integrated with the main machine controls. All such interlocks and permission mechanisms were checked by a team of persons from control, vacuum and front end instrumentation groups. All related operations were declared operational from main control room.

Reported by:

P. Gothwal (pgothwal@rrcat.gov.in), R. P. Yadav, M. Seema, Sanjai Kumar, S. R. Kane, Nilesh Bhang and P. Fatnani

A.7: New Power Supplies for Transport Line-2 Quadrupole Magnets in INDUS

Existing power supplies for quadrupole magnets in TL-2 are based on 6-pulse controlled rectifier and are being continuously used for past several years. These are being replaced with new, compact, efficient and stable power supplies. New, high stability, dc current controlled power supplies of rating 25 V, 80 A have been developed at PSIAD to energize quadrupole magnets in Transport Line-2 (TL-2) of INDUS. They are developed using two switch forward converter topology operating at 50 kHz because of their distinctive merits such as smaller size, lighter weight, better

efficiency, simple configuration, free from shoot through failure, no requirement of demagnetizing winding, high reliability and ruggedness. Input to the power supplies is 415 V, 50 Hz ac while the output voltage and current ratings are 25 V and 80 A respectively. Specified stability of output current is ± 1000 ppm.

Special arrangements have been made during assembly of components to ensure accessibility to failure-prone components for easy maintenance and replacement. Twisted wires have been used for interconnections to minimize stray inductances. The heat dissipation of losses in power devices is transferred through a water cooled heat sink. Wiring has been minimized by using easy pull-out cards with interconnections on the mother board, providing push buttons, test points and LEDs on fascia plate of the cards. In the front end of the dc stage, an in-rush current limit network is incorporated to suppress high surge current during start-up. Each power supply is capable of being operated from local fascia panel or in remote mode from central computer interface via a 25-pin sub-D connector provided on the fascia plate. Various protections like output dc over current, input over current, over temperature of power devices and loss of cooling water flow have been incorporated in design to protect the power supply in case of occurrence of these faults.

Each power supply is housed in a 4U, 19-inch rack as shown in Fig. A.7.1 and they have undergone various tests like:

- Open loop test to check the basic functionality of the power supply.
- Closed loop test to check the stability of control loop.
- Local/Remote operation test which included testing of all the command, status and analog signals both in local as well as in remote mode.
- Heat run test in which power supply is operated continuously for 10 hrs at full rated power output for 5 days.
- Stability test to measure the stability of output current and ensure that it is within specified limits.
- EMI test to measure conducted EMI and ensure that it is as per CISPR-11 standards.

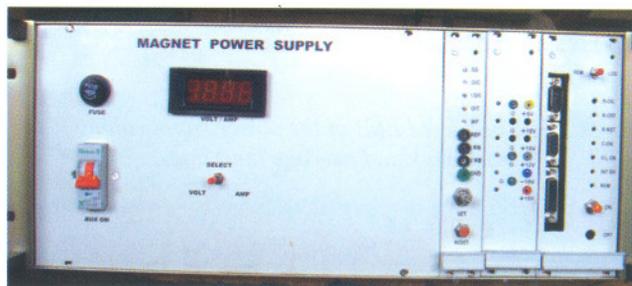


Fig. A.71: Front view of power supply.